5. (Amended) The processing circuit of claim 4, wherein each processing unit comprises a first input terminal to receive the indications of the discrete input values from a processing unit input line common to the processing units and a second input terminal to receive the indications of the discrete input values from another processing unit, the multiplexer coupling the first and second terminals of one of the processing units together to designate the point in the chain at which the accumulation begins.

6. (Amended) The processing circuit of claim 1, wherein each processing unit comprises:

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a first adder circuit to generate an indication of a summation of two of the discrete input values; and

a multiplier circuit coupled to the first adder circuit to generate an indication of a product of a coefficient associated with said each processing unit and the summation of the two discrete values.

7. (Amended) The processing circuit of claim 6, further comprising:

a second adder circuit coupled to the first multiplier circuit to combine the summation of the two discrete input values with a progressive summation provided by another processing unit.

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11. (Amended) The processing circuit of claim 1, wherein the processing units and tap selection circuit comprise at least part of a finite impulse response filter.